REMARKS

Applicants have amended independent Claim 18. Claims 1--20 remain pending.

Objections

Applicants have amended Claim 2 of the present application to obviate the cited objections.

35 U.S.C. Section 103 Rejections

Paragraph 4 of the above referenced Office Action rejects independent Claims 1, 9, and 18 as being rendered obvious by Moreno (US 6,678,795). As such, Applicants respectfully assert that the independent Claims are not rendered obvious by Moreno.

Paragraph 4 of the above reference Office Action states

> "Moreno does not specifically disclose that the order of previous accesses to the two cache lines was not interrupted by other cache line accesses. However, in the case that the pattern was create by a stream type access to the two adjacent cache lines, the access must be sequential in order if those two lines contained stream data. Another entry with Index 183965 in Figure 1 show a similar more elaborate example of a possible stream type access pattern, with 32 adjacent cache lines each assessed only once previously. This could be the result of accessing a longer block " (Page 4, line 17- Page 5, line 2) (emphasis added).

Applicants respectfully point out that all the blocks are accessed in the cited Figure 1 Index and because Moreno does not disclose the order of previous

accesses, Applicants respectfully assert that the Moreno reference does not show or suggest a prefetch apparatus configured "to recognize accesses to a plurality of cache lines, wherein the accesses form a stream type access pattern".

Further, Applicants respectfully direct the Examiner to independent Claim 1 that recites that an embodiment of the present invention is directed to (emphasis added):

> A request tracking data prefetch apparatus for a computer system, comprising:
> a prefetcher coupled to a high latency memory for a processor of the computer system;
> a tracker within the prefetcher and configured to recognize accesses to a plurality of cache lines, wherein the accesses form a stream type access pattern, and use a bit vector to predictively load a target cache line indicated by the stream-type access pattern from the high latency memory into a low latency memory for the processor.

Independent Claim 9 recites distinguishing limitations similar to those recited in Claim 1. Applicants have amended independent 18 to recite a distinguishing limitation similar to that of independent Claims 1 and 9. Applicants assert that the disclosure of Moreno does not disclose or suggest a prefetch unit coupled to a high latency memory. To establish prima facie obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 USPQ 580 (CCPA 1974). (MPEP 2143.03). Applicants have reviewed Moreno and do not understand Moreno to show or suggest a prefetch coupled to a high latency

memory. In contrast, Applicants understand Moreno to show a prefetch engine coupled to a cache controller. Therefore, Applicants respectfully assert that Moreno does not show or teach a prefetch unit coupled to a high latency memory.

Accordingly, Applicants assert that the present invention as recited in independent Claims 1, 9, and 18, is not rendered obvious by Moreno within the meaning of 35 USC Section 103.

CONCLUSION

The Examiner is urged to contact Applicants' undersigned representative if the Examiner believes such action would expedite resolution of the present Application. Please charge any additional fees or apply any credits to our PTO deposit account number: 50-4160.

Respectfully submitted,
MURABITO, HAO & BARNES

Dated: 4/18, 2007

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